IN THE CLAIMS:

1. (Currently Amended) An integrated circuit device comprising:

a semiconductor substrate;

a ~~multilevel~~ metallization interconnect system overlying the semiconductor substrate, ~~each level thereof comprising~~the metallization interconnect system including multiple first interconnect structures located within a dielectric layer;

a bond pad level comprising a ~~plurality of contact pads~~contact pad overlying the metallization interconnect system, ~~one or more of the plurality of contact pads~~the contact pad configured for connection external to the device;

a second interconnect structure ~~connecting one of the plurality of contact pads to a plurality of first interconnect structures~~connected to the contact pad, wherein a portion of the second interconnect structure is disposed in the bond pad level ~~and connected to each one of the plurality of first interconnect structures through a conductive via~~, the second interconnect structure being in physical contact with the multiple first interconnect structures located within the dielectric layer.

2. (Previously Presented) The integrated circuit device of claim 1 wherein a material of the metallization interconnect system comprises copper.

3. (Currently Amended) The integrated circuit device of claim 1 wherein a material of the ~~plurality of contact pads~~contact pad comprises aluminum.

4. (Currently Amended) The integrated circuit device of claim 1 wherein the ~~plurality of contact pads are~~contact pad is configured for connection external to the device by a bond wire attached ~~to one or more of the plurality of contact pads~~thereto.

5. (Currently Amended) The integrated circuit device of claim 1 wherein ~~the plurality of contact pads are~~contact pad is configured for connection external to the device by a solder bump attached ~~to one or more of the plurality of contact pads~~thereto.

6. (Currently Amended) The integrated circuit device of claim 1 wherein a material of the metallization interconnect system comprises copper and the ~~plurality of contact pads~~contact pad comprises aluminum, further comprising a barrier material ~~in regions of physical contact between the copper and the aluminum~~between the copper and the aluminum in regions where the second interconnect structure is in physical contact with the multiple first interconnect structures located within the dielectric layer .

7. (Cancel)

8. (Previously Presented) The integrated circuit device of claim 1 wherein the metallization interconnect system further comprises substantially horizontal conductive runners and substantially vertical conductive vias interconnecting overlying and underlying conductive

runners.

9. (Previously Presented) The integrated circuit device of claim 8 wherein a material of the substantially horizontal conductive runners and the substantially vertical conductive vias comprises copper.

10. (Currently Amended) The integrated circuit device of claim 1 further comprising a passivation layer disposed between ~~the bond pad level and the metallization interconnect system, wherein the passivation layer is further disposed between~~ the second interconnect structure and ~~an uppermost level of the metallization interconnect system~~the dielectric layer.

11. (Original) The integrated circuit device of clam 1 further comprising a passivation layer overlying the bond pad level.

12. (Previously Presented) An integrated circuit device comprising:

a ~~multilevel~~ metallization interconnect system located over a substrate~~, each level thereof comprising first interconnect structures~~, the metallization interconnect system including multiple first interconnect structures located within a dielectric layer;

a plurality of contact pads disposed over ~~an uppermost level of the multilevel~~the metallization interconnect system, one or more of the plurality of contact pads configured for connection external to the device; and

a second interconnect structure coplanar with at least one of the plurality of contact pads and electrically connected thereto, the second interconnect structure comprising a plurality of conductive elements ~~each connected to one of the first interconnect structures through a conductive via~~physically contacting the multiple first interconnect structures.

13. (Currently Amended) The integrated circuit device of claim 12 wherein a material of the ~~multilevel~~ metallization interconnect system comprises copper.

14. (Previously Presented) The integrated circuit device of claim 12 wherein a material of the contact pads and the second interconnect structure comprises aluminum.

15. (Currently Amended) The integrated circuit device of claim 12 wherein the ~~multilevel~~ metallization interconnect system comprises substantially horizontal conductive runners and substantially vertical conductive vias interconnecting overlying and underlying conductive runners.

16. (Currently Amended) The ~~Integrated~~ integrated circuit device of claim 15 wherein a material of the substantially horizontal conductive runners and the substantially vertical conductive vias comprises copper.

Claims 17-25 (Canceled)

26. (Previously Amended) The integrated circuit of claim 1 wherein at least a portion of the second interconnect structure is disposed above ~~one or more of the plurality of contact pads~~the contact pad.

27. (New Claim) The integrated circuit of Claim 1 wherein the second interconnect structure is a power bus.

28. (New Claim) The integrated circuit of Claim 12 wherein the second interconnect structure is a power bus.